A Comparison of the New PC Riser Specifications

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Purpose of this White Paper

The Communication and Networking Riser (CNR) and the Advanced Communication Riser (ACR) specifications both define a type of PC riser card, with similar goals, but very different approaches. The purpose of this white paper is to explore and compare the major differences between these specifications.

1. Introduction

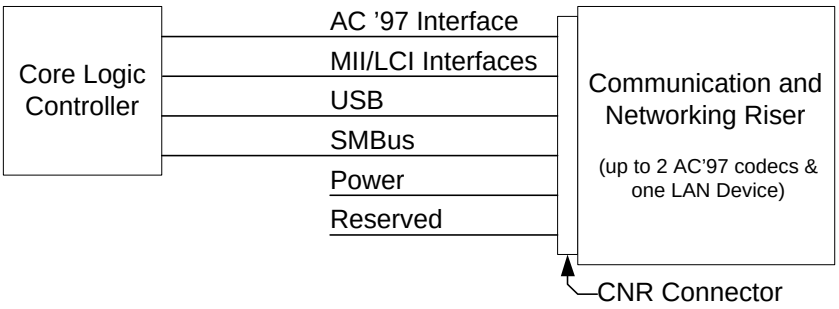
Over the last two years, the PC industry has developed a need for riser architecture to reduce the overall system cost and increase the flexibility of the system manufacturing process. The Audio/Modem Riser (AMR) specification, introduced in July 1998, was the beginning of a new riser architecture approach. AMR had the capability to support both audio and modem functions. However, it did have some shortcomings, which were identified after the release of the specification. These shortcomings included the lack of Plug and Play (PnP) support, as well as the consumption of a PCI connector location. Recently, new riser architecture specifications have been defined which combine more functions onto a single card. These new riser architectures combine audio, modem, broadband technologies, and Local Area Network (LAN) interfaces onto a single card. They continue to give motherboard Original Equipment Manufacturers (OEM) the flexibility to create a generic motherboard for a variety of customers. The riser card allows OEM's and system integrators to provide a customized solution for each customer's needs. The two most recent riser architecture specifications include the CNR and ACR.

2. CNR Overview

The CNR specification is an open riser architecture and is currently available at http://developer.intel.com/technology/cnr/ .

The CNR Specification supports five interfaces, AC'97, Universal Serial Bus (USB), System Management Bus (SMBus), and two LAN interfaces (Lan Connect Interface (LCI) and Media Independent Interface (MII)). Each CNR card can utilize a maximum of four interfaces by choosing the specific LAN interface to support. Please refer to Figure 1.

Figure 2-1. Communication and Networking Riser Card



A description of the interfaces are listed below:

- AC '97 Interface – Supports audio and modem functions on the CNR card.
- Lan Connect Interface (LCI) – Provides 10/100 LAN or Home Phoneline Networking capabilities for Intel chipset based solutions (refer to the CNR specification).
- Media Independent Interface (MII) – Provides 10/100 LAN or Home Phoneline Networking capabilities for CNR platforms using the MII Interface.
- Universal Serial Bus (USB) – Supports new or emerging technologies such as DSL or wireless.
- System Management Bus (SMBus) – Provides Plug and Play (PnP) functionality on the CNR card.

3. ACR Overview

Due to the lack of a publicly available version of the Advanced Communication Riser (ACR) Specification, all information contained in this paper regarding the ACR Specification has been obtained from documents available on the ACR Special Interest Group (SIG) website (http://www.acrsig.org/) and presentations made at the Platform Conference. The differences listed below between the two riser specifications are a compilation of information gathered via the references above.

Although ACR has similar functionality to the CNR specification, the ACR implementation is very different. ACR implementation is as follows:

- Use existing PCI connector
- Replace ISA Edge Slot
- Backwards compatible to AMR
- Two MAC/PHY interface ports
- Integrated Packet Bus (IPB) for DSL
- Supports future wireless technology

4. Implementation Differences

As described in the previous section, there are several architectural differences between the CNR Specification and the ACR Specification. The following sections will analyze these differences in more detail.

1. Use of a PCI connector slot as opposed to the shared slot strategy of CNR:

   Small ATX form factor boards, like microATX, may find the ACR architecture of losing a PCI connector an unacceptable trade-off, as compared to the CNR architecture of a shared connector.

2. Backward compatibility with AMR:

   The ACR support for backwards compatibility with AMR has the potential to be valuable. However, adding support for the low attach rate riser may be at the expense of consuming a PCI connector slot and increased Windows Hardware Quality Labs (WHQL) testing support and cost.

3. IPB versus USB:

   The ACR-developed IPB provides the capability to support xDSL technologies. The down side is that it requires the development of a new interface, along with the associated silicon, drivers, and validation resources. The CNR specification supports xDSL technologies through the existing, stable USB interface, already available in today's core logic chipsets.

4. Multiple MII Interfaces:

   The ACR support for multiple MII interfaces does provide an architecture that supports a potential market of combined Wide Area Network (WAN)/LAN riser cards. However it does this at the expense of requiring multiple MII host controllers, or MAC's, on the motherboard (or integrated into the chipset). The CNR Specification also supports the same combined WAN/LAN card, but through system architecture, that utilizes existing interfaces and chipset architectures, without adding excessive cost to the board for a small market.

5. Future Wireless Interface:

   Both the ACR SIG and CNR understand the need to support wireless technologies in the future. The ACR Specification has already reserved pins for a future wireless interface. The CNR Specification has the pins available to support a wireless interface, if justified by attach rates. These pins will be defined as the wireless market becomes more mature.

6. Open Industry Specification:

   The CNR is truly an open industry specification. The specification is available to anyone that wishes to download it. There are no membership requirements, no NDA's to be signed, and no royalty payments.

These differences clearly separate CNR and ACR from each other. Each issue will be discussed in more detail.

4.1. PCI Slot & ISA Edge Slot Issues

Like the original AMR Specification, the ACR Specification was designed to occupy or replace an existing PCI connector slot. This effectively reduces the number of available PCI slots by one, regardless of whether the ACR connector is used. Though this may be acceptable in a larger form factor motherboard, such as ATX, the loss of a PCI connector in a microATX or FlexATX motherboard is generally viewed as an unacceptable tradeoff. In these smaller form factors, there may be as few as two expansion slots available. Dedicating one of those slots to an ACR connector leaves only a single expansion slot for end user or system integrator upgrade.

The CNR specification over-comes this issue by implementing a shared slot strategy, much like the shared ISA/PCI slots of the very recent past. In a shared slot strategy, both the CNR and PCI connectors effectively use the same I/O bracket space. Unlike the ACR architecture, when the system integrator chooses not to use a CNR card, the shared PCI slot is still available. In the two-slot microATX motherboard, the CNR Specification strategy allows the maximum number of expansion slots, while still allowing for flexibility and cost reductions through the use of riser cards.

The ACR SIG position is that the loss of a PCI expansion slot is of little concern as the potential functions that can be placed on an ACR card far outweigh the loss of the PCI expansion slot. This may be true in a few instances, but the OEM and system integrators must carefully weigh the loss of this slot against the availability of riser cards and associated feature sets to be implemented in a given system.

The ACR SIG also states that by using a “highly adopted PCI connector”, the overall system cost is reduced. This may have been a true statement at the time it was written, however, Intel’s analysis of the connector market shows that the 60-pin CNR connector and the standard 120-pin PCI connector are currently at price parity. In addition, if one were to analyze the “should cost” models, the CNR connector cost will decrease below that of a PCI connector as the CNR connector volumes increase.

Finally, the statement regarding replacing the ISA Edge slot must be carefully weighed. Since the ACR connector must be spaced 0.8 inches (20.32mm) from the adjacent PCI connector (where the ISA connector is spaced 0.605 inches or 15.37mm from the adjacent PCI connector), there may be instances where the motherboard will need to be extended. This has ramifications in both increased circuit board cost and potential chassis size issues (if the extended board size required to support the ACR connector causes the motherboard size to increase beyond capabilities of the chassis).

4.2. Backward Compatibility with AMR

ACR was designed to be backward compatible with current AMR designs. Compatibility with AMR can create many implementation issues.

First, obtaining WHQL support can be a difficult and costly process. The multiple architectures (AMR and ACR) require different WHQL submission models, making the validation process long and complicated. Once the new riser architectures gain wide acceptance, it is entirely possible that WHQL will no longer support the older riser architectures, especially with the lack of PnP support on AMR.

Second, PnP is an issue for existing AMR designs. Although the lack of PnP support on AMR was not the primary reason for CNR breaking backward compatibility, it does help to ensure that a PnP compatible riser card is installed in the system, thus helping to ensure that the correct drivers are loaded by the Operating System (OS).

4.3. A new Integrated Packet Bus (IPB) vs. the Universal Serial Bus (USB)

ACR proposes IPB as a new interface for DSL. The IPB architecture is very similar to the MAC/PHY architecture of the LAN world, in that a host controller and an Analog Front End (AFE) are required. The IPB host controller can either be integrated in the chipset or placed as a discrete component on the motherboard. Integration into the chipset will cause a corresponding increase in the chipset price. Until the attach rate for DSL reaches 40 to 50% this solution would not be cost effective (why would a motherboard manufacturer want to pay for a feature they won't use?). For IPB to be integrated, another controller must be added to the chipset. According to several design engineers, this can increase the core logic die size up to 40%.

IPB is not needed as DSL can be supported in other ways, such as through USB. The CNR specification states that USB is the appropriate interface to implement emerging technologies in a riser architecture, as it contains all of the necessary PnP protocol and adequate bandwidth (especially with the introduction of USB2.0). Aside from the questionable need for a low attach rate interface, the development path of the IPB is an issue to consider. An entire silicon infrastructure needs to be developed around IPB, including host controllers or chipsets, AFE, and supporting circuitry. When this silicon development effort is combined with the need for validation of host controller and AFE interoperability, as well as software driver development and industry adoption, it becomes obvious that the IPB is not worth the development effort when it is focused on a single, low attach rate technology. Once DSL attach rates increase, it would make sense to visit the idea of a dedicated interface.

4.4. ACR's Multiple MII Interfaces

The ACR Specification supports two MII interfaces. The ACR SIG website suggests that these two MII interfaces can be used to support simultaneous WAN and LAN, for example a Cable Modem and 10/100 Ethernet. Though this is possible with the ACR architecture, there are some issues to consider. Specifically, what is the cost of support for two MII controllers either integrated in the chipset or placed on the motherboard, and is the additional cost justified by the attach rate? Additionally, are the pins added to the ACR connector to support these interfaces effectively reducing the motherboard space available for other features or required trace routing?

The CNR architecture also supports both a WAN and LAN through a platform architecture that is common and inexpensive. As previously mentioned, the CNR specification supports USB as well as either the LCI or the MII interface. The USB connection support the WAN requirement through Cable Modem or DSL, while the LCI/MII interface(s) support the LAN requirement, through 10/100 Ethernet. All of these interfaces are supportable on today's chipsets, without the requirement to unnecessarily increase the system cost for a small market segment. This support is provided through a smaller connector, thus reducing the overall system cost.

4.5. Future Wireless Interface

Wireless technologies are beginning to increase in availability, potentially becoming a high attach rate feature. Both the ACR SIG and CNR specification have recognized this and have addressed riser support through different means. The ACR SIG has dedicated a section of the ACR connector specifically for future support of a wireless interface. The CNR Specification contains several reserved pins, which can be defined in the future for wireless, if warranted. The current CNR position is the

assignment of reserved pins to a wireless interface is premature. This is due to the fact that the wireless attach rate is extremely low and there are many different standards for wireless technologies. The two factors combined will make standardizing a wireless interface very difficult.

As stated previously, the CNR Specification supports emerging technologies, such as wireless, using the USB interface on the CNR connector.

4.6. Open Industry Specification

The ACR SIG has stated, in many instances, that the ACR Specification is an open industry standard while CNR is a proprietary specification. A more detailed analysis of the actual availability of the specification reveals a slightly different story.

The ACR Specification is only available to an interested party by joining the ACR SIG. Part of joining the ACR SIG requires the signing of a Non-Disclosure Agreement (NDA). Without joining the ACR SIG and signing the NDA, the ACR specification cannot be received.

The CNR Specification, however, has been available to the entire industry since early February of 2000, by simply downloading the specification from the CNR website

http://developer.intel.com/technology/cnr/

5. Summary

Both the CNR and ACR Specifications address the increasing need for a riser architecture and both specifications have addressed this architecture in different ways. The ACR SIG has chosen to implement a set of features that have questionable value. Some of these include the following:

- Use of a PCI connector slot as opposed the shared slot strategy of CNR
- Backward compatibility with AMR
- IPB versus USB
- Multiple MII Interfaces
- Future Wireless Interface
- No Open Industry Specification

In addition to the above points, one must also consider how riser architecture supports the chipsets available today and in the future. CNR supports both Intel and non-Intel chipsets. The ACR Specification may support non-Intel chipsets, but it does NOT support the full feature set of today's Intel chipsets.

Ultimately, the motherboard manufacturer must make the best decision for their specific customers and their specific business model. This may mean that one riser specification is chosen over another. However, it is best to weigh all of the trade-offs and their long-term implications, ultimately leading to an informed decision.

Questions regarding this white paper may be sent to cnr.support@intel.com.